IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Weixun Cao
Title:	DIRECT MODULATION OF A POWER AMPLIFIER WITH ADAPTIVE DIGITAL PREDISTORTION
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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Response to Final Office Action

Dear Sir:

In response to Final Office Action dated 02/20/2006, the Applicant respectfully requests the Examiner to enter the amendments as follows:

AMENDMENTS TO THE SPECIFICATION begin on page 2 of this Response

AMENDMENTS TO THE CLAIMS are reflected in the listing of claims which begins on page 4 of this Response.

REMARKS begin on page 10 of this Response.

AMENDMENTS TO THE SPECIFICATION

1. Please amend paragraph [0035] as follows:

[0035] At the same time, the phase signal PM2 is also applied to the phase offset **523** for the fractional-N PLL modulation **500** that is used to track the carrier frequency of VCO **521**. In operation, a modulated signal from the loop filter **517** is coupled to the adder **519** such that the VCO **521** operates with two signals. By using the feed-forward phase modulation through the D/A converter **513**, a change in the phase gain value will result in an equivalent change in the modulation gain of VCO **521**. Thus, the nonlinear effect of VCO gain drift can be adaptively compensated by predistorting the scaling value of the phase gain **511**. Also, a controller **524** receives the phase-modulated baseband signal and the carrier frequency signal to produce a ~~digital bit stream used~~ signal to control a reference frequency coupled to an input of the phase detector **515**.

2. Please amend paragraph [0037] as follows:

[0037] According to one embodiment, the fractional-N phase-locked loop (PLL) frequency synthesizer **500** is used as a functional building block in the transmitter **580**. The phase-locked loop **500** includes a phase detector **515**, a loop filter **517**, a voltage controlled oscillator (VCO) **521** and a loop divider **525**. The phase detector **515** serves as a comparator ~~means~~ for comparing the signal from the controller **524** ~~reference signal f_{ref}~~ to the divided loop output signal ~~which is coupled to the output of~~ from the divider **525**. The phase detector **515** generates a frequency tuning control signal that is coupled to the loop filter **517**. The voltage level of this frequency tuning control signal is proportional to the difference in frequencies of the compared signals. The loop filter **517** receives and filters the frequency tuning control signal and provides a control signal to the input node **519** to the VCO **521**. The VCO **521** serves as a frequency generation means for generating the loop output signal f_{out} in response to the VCO input control signal. The loop divider **525** is coupled to the output of the VCO **521** and generates a divided loop signal which corresponds to the frequency to the loop output signal divided by integer N or N+1. The output of the

loop divider **525** is provided as the loop feedback signal to the other input of phase detector **515**.

AMENDMEND TO CLAIMS

Please amend claims 4, 11, 14-15, and 17-23 as following:

1. (*Previously amended*) A transmitter operating in a switching-mode, the transmitter comprising:

a signal decomposition unit decomposing a modulated digital signal into a first signal and a second signal, both being expressed in polar coordinates;

an adaptive predistorter distorting the first and second signals respectively in accordance with one or more of distorting parameters;

a phase equalizer equalizing a time delay between the first and second signals in response to a measurement provided by a feedback loop operating on a sample of a RF signal from the transmitter; and

a power amplifier, controlled by the first signal and a phase-modulated signal coupled from a voltage controlled oscillator, producing the RF signal.

2. (*Original*) The transmitter of claim 1, wherein the modulated digital signal is provided from a baseband processor, the first signal is an amplitude signal, and the second signal is a phase signal, and the phase-modulated signal is produced from the second signal.

3. (*Original*) The transmitter of claim 2, wherein the feedback loop includes a down-converter, a demodulation unit and a measurement unit, and provides feedback signals to at least the phase equalizer.

4. (*Currently amended*) The transmitter of claim 3, ~~wherein the down-converter converts the sample to a lower frequency to be demodulated in the demodulation unit, and the demodulated sample is measured in the measurement unit for producing the feedback signals~~ further comprising converting the sample to a lower frequency to be demodulated in the demodulation unit to produce a demodulated sample, wherein the

demodulated sample is measured in the measurement unit for producing the feedback signals.

5. (*Original*) The transmitter of claim 1, wherein the first signal is provided to indirectly control the power amplifier.

6. (*Original*) The transmitter of claim 5, wherein the first signal activates a control unit to generate a bias control signal and a voltage signal in response to the first signal.

7. (*Original*) The transmitter of claim 5, further comprising a first modulation path and a second modulation path, both operating on the second signal.

8. (*Original*) The transmitter of claim 7, wherein the first modulation path provides a first input signal to the voltage controlled oscillator in response to the second signal processed in a phase gain unit.

9. (*Original*) The transmitter of claim 8, wherein the second signal, after processed in the phase gain unit, is converted to an analog signal.

10. (*Previously amended*) The transmitter of claim 8, wherein the second modulation path provides a second input signal to the voltage controlled oscillator in response to the second signal processed in a phase offset unit.

11. (*Currently amended*) The transmitter of claim 10, wherein the second modulation path is formed by a phase-locked loop (PLL) including an adder that couples ~~both the first input signal and second input signal~~ an output of a loop filter with a phase gain to modulate the voltage controlled oscillator.

12. (*Previously amended*) A method for controlling a transmitter to operate in a switching-mode, the method comprising:

decomposing a modulated digital signal into a first signal and a second signal, both being expressed in polar coordinates;

distorting the first and second signals respectively in accordance with one or more of distorting parameters;

equalizing a time delay between the first and second signals in response to a measurement provided by a feedback loop operating on a sample of a RF signal from the transmitter; and

producing the RF signal in a power amplifier controlled by the first signal and a control signal coupled from a voltage controlled oscillator.

13. (*Original*) The method of claim 12, wherein the modulated digital signal is provided from a baseband processor, the first signal is an amplitude signal, and the second signal is a phase signal, and the control signal is produced from the second signal.

14. (*Currently amended*) The method of claim 12, ~~wherein the feedback loop includes a down-converter, a demodulation unit and a measurement unit, and provides feedback signals to at least a phase equalizer~~ further comprising providing feedback signals by the feedback loop to at least a phase equalizer, the feedback loop formed by a down-converter, a demodulation unit and a measurement unit.

15. (*Currently amended*) The method of claim 14, ~~wherein the down-converter converts the sample to a lower frequency to be demodulated in the demodulation unit, and the demodulated sample is measured in the measurement unit for producing the feedback signals~~ further comprising converting the sample to a lower frequency to be demodulated in the demodulation unit to produce a demodulated sample, wherein the demodulated sample is measured in the measurement unit for producing the feedback signals.

16. (*Original*) The method of claim 12, wherein the first signal is provided to indirectly control the power amplifier.

17. (*Currently amended*) The method of claim 16, ~~wherein the first signal activates a control unit to generate a bias control signal and a voltage signal in response to the first signal~~ further comprising activating a control unit by the first signal to generate a bias control signal and a voltage signal in response to the first signal.

18. (*Currently amended*) The method of claim 16, ~~wherein the transmitter comprises a first modulation path and a second modulation path, both operating on the second signal~~further comprising a first modulation path and a second modulation path, both operating on the second signal.

19. (*Currently amended*) The method of claim 18, ~~wherein the first modulation path provides a first input signal to the voltage controlled oscillator in response to the second signal processed in a phase gain unit~~ further comprising providing a first input signal by the first modulation path to the voltage controlled oscillator in response to the second signal processed in a phase gain unit.

20. (*Currently amended*) The method of claim 19, ~~wherein the second signal, after processed in the phase gain unit, is converted to an analog signal~~ comprising converting the second signal, after processed in the phase gain unit, to an analog signal.

21. (*Currently amended*) The method of claim 19, ~~wherein the second modulation path provides a second input signal to the voltage controlled oscillator in response to the second signal processed in a phase offset unit~~ further comprising providing a second input signal in the second modulation path to the voltage controlled oscillator in response to the second signal processed in a phase offset unit.

22. (*Currently amended*) The method of claim 21, ~~wherein the second modulation path is formed by a phase-locked loop (PLL) including an adder that couples both the first and second input signals to modulate the voltage controlled oscillator~~ further

comprising forming the second modulation path by a phase-locked loop (PLL) that is formed by an adder adding an output of a loop filter with a phase gain to modulate the voltage controlled oscillator.

23. (*Currently amended*) A method for controlling a transmitter to operate in a switching-mode, the method comprising:

compensating a frequency drift and other non-linear effects of a modulated voltage-controlled-oscillator (VCO) and a power amplifier by predistorting a baseband amplitude signal and a phase signal in accordance with one or more distorting parameters that are determined based on a sample of an output of the transmitter, wherein the baseband amplitude signal and the phase signal have been decomposed in terms of polar coordinates;

providing a phase-locked loop (PLL) with an adaptive phase gain and a phase offset control in response to the phase signal; ~~and~~

modulating the power amplifier with the baseband amplitude signal and an output coupled from the modulated voltage controlled oscillator (VCO).

24. (*Original*) The method of claim 23, further comprising:

demodulating samples of an output of the power amplifier and the modulated voltage controlled oscillator to regenerate a first signal, a second signal and a third signal in a digital format;

comparing the demodulated first and second signals to the baseband amplitude signal and phase signals with reference to the third signal, respectively; and

producing feedback control signals to update the one or more distorting parameters, and other related parameters.

25. (*Original*) The method of claim 24, still further comprising equalizing a delay time between the baseband amplitude and phase signals.

26. (*Original*) The method of claim 25, wherein the delay time is provided by one of the feedback control signals.

27. (*Currently amended*) The method of claim 23, wherein the phase-locked loop (PLL) comprises:

the voltage-controlled oscillator (VCO) with a control input and a phase-modulated output;

a phase detector to compare two phase-modulated signals and produce an output representing the phase difference of the two phase-modulated signals;

a loop filter coupled to the output of the phase detector and to the input of the VCO;

a feedback loop including a feedback frequency divider which is coupled to the output of the VCO ~~and to an input of the phase detector~~;

a reference frequency signal coupled to another input of the phase detector; and

a modulator receiving a signal from an adder that couples a phase-modulated baseband signal and a carrier frequency signal together to produce a digital bit stream used to control a divisor of the feedback frequency divider.

28. (*Previously amended*) The method of claim 23, wherein a controller receives a phase-modulated baseband signal and a carrier frequency signal to produce a digital bit stream used to control a reference frequency coupled to an input of a phase detector.

29. (*Currently amended*) The method of claim 23, wherein the VCO operates by:

coupling the phase-modulated baseband signal to an input node of the VCO which is used by the phase-locked loop;

using an adaptive phase gain to scale the phase-modulated baseband signal before being coupled to the input node of the VCO of the phase-locked loop;

using an adaptive phase offset to change the phase-modulated baseband signal which is ~~applied~~ coupled to the input of a controller of ~~a~~ the phase locked loop; and

using adaptive digital predistortion to generate the adaptive phase gain and phase offset signals.

REMARKS

Claims 1 - 29 were submitted for examination. In this Office Action, Claims 1-3, 5-10, 12-13 and 16 are allowed, claims 4, 11, 14-15, and 17-22 are rejected under 35 USC 112, and claims 23-29 are rejected under 35 USC(a) as being unpatentable over Sander et al (US Pat. App. Pub. No.: 20040208157, hereinafter "Sander") in view of Minoda et al (US Pat. No.: 5,661,425, hereinafter "Minoda").

The Examiner is appreciated for the thoughtful examination and comments in the Office Action. In the foregoing amendments, the Applicant has amended the specification to clarify the question raised by the Examiner on page 3 of the Office Action, and Claims 4, 11, 14-15, and 17-22 to correct the informalities raised by the Examiner. The Applicant submits that no new matters have been added. Accordingly, the Applicant believes that the rejections under 35 USC 112 have been overcome. Claims 1-22 shall be now in condition for allowance.

Patentability of Claim 23:

Claims 23-29 are still rejected. Claim 23 has been amended to include a limitation shown in FIG. 5. It is axiomatic that an invention in a patent application is defined by, and must be examined with respect to, the specific language of the claims. As amended, Claim 23 now recites:

> compensating a frequency drift and other non-linear effects of a modulated voltage-controlled-oscillator (VCO) and a power amplifier by predistorting a baseband amplitude signal and a phase signal in accordance with one or more distorting parameters <u>that are determined based on a sample of an output of the transmitter</u>, wherein the baseband amplitude signal and the phase signal have been decomposed in terms of polar coordinates;
>
> providing a phase-locked loop (PLL) with an adaptive phase gain and a phase offset control in response to the phase signal; and
>
> modulating the power amplifier with the baseband amplitude signal and an output coupled from the modulated voltage controlled oscillator (VCO).

(*emphasis added*)

FIG. 5 of the instant application clearly shows that a sample of the output of the transmitter is taken and goes through a down-conversion unit 537 and a demodulation 535 to determine the predistortion calibration. In other words, there is a feedback loop including the output of the transmitter.

In contrast, Sander shows in FIG. 12 that no sample of the output is taken to control the “pre-distortion” of the signals. In other words, Sander fails to teach nor suggest a feedback loop including the output of the transmitter, neither does Minoda teach such, viewed alone or in combination. Accordingly, the Applicant respectfully submits Claim 23 shall be allowable over the cited references. Reconsideration of Claims 23-29 is respectfully requested.

In view of the above amendments and remarks, the Applicant believes that Claims 1 - 29 shall be in condition for allowance over the cited references. Early and favorable action is being respectfully solicited.

If there are any issues remaining which the Examiner believes could be resolved through either a Supplementary Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned at (408)777-8873.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to "Commissioner of Patents and Trademarks, Washington, DC 20231", on May 21, 2007.

e-filed

Signature: / joe zheng /
Joe Zheng

Respectfully submitted;

/ joe zheng /

Joe Zheng
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